

What is claimed is:

1 1. A test circuit for a logical integrated circuit,
2 comprising:

3 plural flip-flops of a scanning type (FFs, hereinafter)
4 arranged in first to nth stages, in each of which said FFs are
5 successively connected in series,

6 plural logic gates, output terminals of which are
7 respectively connected with input terminals of said plural FFs,
8 and

9 a scan path which is formed of a series connection of a part
10 or a whole of said plural FFs, and propagates a test pattern for
11 measuring an alternating current (AC, hereinafter) characteristic
12 of an input or output terminal of said logical integrated circuit,

13 wherein said scan path connects an output terminal of said
14 FF standing at an end of said first stage with a scan output.

1 2. A test circuit for logical integrated circuit,
2 comprising:

3 plural FFs arranged in first to nth stages, in each of which
4 said FFs are successively connected in series,

5 plural logic gates, output terminals of which are
6 respectively connected with input terminals of said plural FFs,
7 and

8 a scan path which is formed of a series connection of a part
9 or a whole of said plural FFs, and propagates a test pattern for
10 measuring an AC characteristic of an input or output terminal of
11 said logical integrated circuit,

12 wherein said scan path connects a scan input with an input
13 terminal of said FF standing at a head of said n th stage.

1 3. A test circuit for a logical integrated circuit,
2 comprising,
3 plural FFs arranged in first to n th stages, in each of which
4 said FFs are successively connected in series,
5 plural logic gates, output terminals of which are
6 respectively connected with input terminals of said plural FFs,
7 and

8 a scan path which is formed of a series connection of a part
9 or a whole of said plural FFs, and propagates a test pattern for
10 measuring an AC characteristic of an input or output terminal of
11 said logical integrated circuits,

12 wherein said scan path connects a scan input with an input
13 terminal of said FF standing at a head of said n th stage,

14 again successively connects said FFs arranged in said second
15 to (n-1) th stages in series, after restarting from an output
16 terminal of said FF standing at an end of said n th stage,

17 once again connects an output terminal of said FF standing
18 at an end of said (n-1) th stage with an input terminal of said
19 FF standing at a head of said first stage, and

20 finally connects an output terminal of said FF standing at
21 an end of said first stage with a scan output.

1 4. A method for testing a logical integrated circuit, which
2 is compose of:

3 plural FFs arranged in first to n th stages, in each of which

4 said FFs are successively connected in series,

5 plural logic gates, output terminals of which are
6 respectively connected with input terminals of said plural FFs,
7 and

8 a scan path which is formed of a series connection of a part
9 or a whole of said plural FFs, and propagates a test pattern for
10 measuring an AC characteristic of an input or output terminal of
11 said logical integrated circuit, comprising the steps of:

12 connecting an output terminal of said FF standing at an end
13 of said first stage with a scan output,

14 inputting a clock signal to a clock signal input terminal,
15 inputting a predetermined data signal to one of said input
16 terminals of said logical integrated circuit, and

17 measuring said AC characteristic of said one of said input
18 terminals of said logical integrated circuit by inspecting an
19 output of said scan output.

1 5. A method for testing a logical integrated circuit, which
2 is composed of:

3 plural FFs arranged in first to n th stages, in each of which
4 said FFs are successively connected in series,

5 plural logic gates, output terminals of which are
6 respectively connected with input terminals of said plural FFs,
7 and

8 a scan path which is formed of a series connection of a part
9 or a whole of said plural FFs, and propagates a test pattern for
10 measuring an AC characteristic of an input or output terminal of
11 said logical integrated circuit, comprising the steps of:

12 connecting a scan input with an input terminal of said FF
 13 standing at a head of said n th stage,
 14 inputting a clock signal to a clock signal input terminal,
 15 inputting a predetermined data signal to a scan input, and
 16 measuring an AC characteristic of one of said output
 17 terminals of said logical integrated circuit by inspecting an
 18 output of said one of said output terminals.

1 6. A method for testing a logical integrated circuit, which
 2 is composed of:

3 plural FFs arranged in first to n th stages, in each of which
 4 said FFs are successively connected in series,

5 plural logic gates, output terminals of which are
 6 respectively connected with input terminals of said plural FFs,
 7 and

8 a scan path which is formed of a series connection of a part
 9 or a whole of said plural FFs, and propagates a test pattern for
 10 measuring an AC characteristic of an input or output terminal of
 11 said logical integrated circuit, comprising the steps of:

12 connecting a scan input with an input terminal of said FF
 13 standing a head of said n th stage,

14 connecting said FFs arranged in said second to (n-1) th
 15 stages successively in series, after restarting from an output
 16 terminal of said FF standing at an end of said n th stage,

17 connecting an output terminal of said FF standing at an end
 18 of said (n-1) th stage with an input terminal of said FF standing
 19 at a head of said first stage,

20 connecting an output terminal of said FF standing at an end

21 of said first stage with a scan output,
22 inputting a clock signal to a clock signal input terminal,
23 inputting a predetermined data signal to one of said input
24 terminals of said logical integrated circuit, and
25 measuring said AC characteristic of said one of said input
26 terminals of said logical integrated circuit by inspecting an
27 output of said scan output.

1 7. A method for testing a logical integrated circuit, which
2 is composed of:

3 plural FFs arranged in first to n th stages, in each of which
4 said FFs are successively connected in series,

5 plural logic gates, output terminals of which are
6 respectively connected with input terminals of said plural FFs,
7 and

8 a scan path which is formed of a series connection of a part
9 or a whole of said plural FFs, and propagates a test pattern for
10 measuring an AC characteristic of an input or output terminal of
11 said logical integrated circuit, comprising the steps of:

12 connecting a scan input with an input terminal of said FF
13 standing a head of said n th stage,

14 connecting said FFs arranged in said second to (n-1) th
15 stages successively in series, after restarting from an output
16 terminal of said FF standing at an end of said n th stage,

17 connecting an output terminal of said FF standing at an end
18 of said (n-1) th stage with an input terminal of said FF standing
19 at a head of said first stage,

20 connecting an output terminal of said FF standing at an end

21 of said first stage with a scan output,
22 inputting a clock signal to a clock signal input terminal,
23 inputting a predetermined data signal to a scan input, and
24 measuring an AC characteristic of one of said output
25 terminals of said logical integrated circuit by inspecting an
26 output of said one of said output terminals.

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